REMARKS

Claims 1-10 are pending in this application, with claims 2-8 having been withdrawn from consideration pursuant to a restriction requirement. Applicants have amended claim 1 for clarity, and have entered new claims 9 and 10 to cover additional aspects of the invention. Reconsideration and allowance of this application are respectfully requested in view of the above amendments and the following remarks.

Claim 1 is rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Kinoshita, U.S. Patent No. 6,127,633, in view of Miles et al., U.S. Patent No. 5,535,101, and Arai et al., U.S. Patent No. 5,315,072. Applicants respectfully traverse this rejection for at least the following reasons.

In making this rejection, the Examiner admits that Kinoshita does not disclose "the specifics of the conductor mounting to an integrated circuit chip and the use of a dummy circuit beneath the interlaminar layer." The Examiner asserts that these features are found in Miles et al. and Arai et al. Applicants respectfully disagree with these assertions.

Applicants submit that none of the cited references, either alone or in any proper combination, discloses or suggests all of the advantageous features recited in claim 1 and new claims 9 and 10. In particular, Applicants disagree with the Examiner's assertion that Arai et al. discloses a "dummy pattern" as recited in claims 1, 9, and 10. On page 27, lines 17-19 of the instant specification, the term "dummy pattern" is defined as "a pattern formed just mechanically; [having] no functional meaning such as an electric connection, capacitor, etc." While the dummy pattern has no electrical "functional meaning," it is mechanically useful.

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As is explained on page 7, lines 23-25 of the Specification, the "metallic dummy pattern...is effective to improve the mechanical strength of the outer periphery of the package board, as well as protect the package board from warping."

By contrast, Applicants note that Arai et al. defines element 27 as an "inner layer conductor," an element that is electrically connected. (See Arai et al. at column 3, lines 50-54 and lines 59-62.) Accordingly, Applicants submit that neither Arai et al. nor any of the other cited references discloses a "dummy pattern."

Since none of the cited references discloses or suggests a package board having a "dummy pattern" as recited in claims 1, 9, and 10, Applicants respectfully submit that the subject matter of those claims would not have been obvious over the cited combination of references. Therefore, Applicants respectfully request the rejection be withdrawn.

In view of the foregoing, Applicants respectfully submit that this application is in condition for Allowance, and timely Notice to that effect is earnestly solicited. If questions relating to patentability remain, the Examiner is invited to contact the undersigned to discuss the same.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 1 is amended as follows:

1. A package board having a core board on each surface of which a plurality of conductor circuits are formed with an interlaminar resin insulating layer therebetween, wherein a plurality of soldering pads are formed on the IC chip mounted side surface, as well as on the other side surface to be connected to another board, so that said soldering pads on the other side surface are larger than those on said IC chip side surface of said package board, and

a dummy pattern for improving the mechanical strength of the package board is formed between signal line conductor circuit patterns formed on said IC chip mounted side surface of said core board.

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